OXFORD INSTRUMENTS

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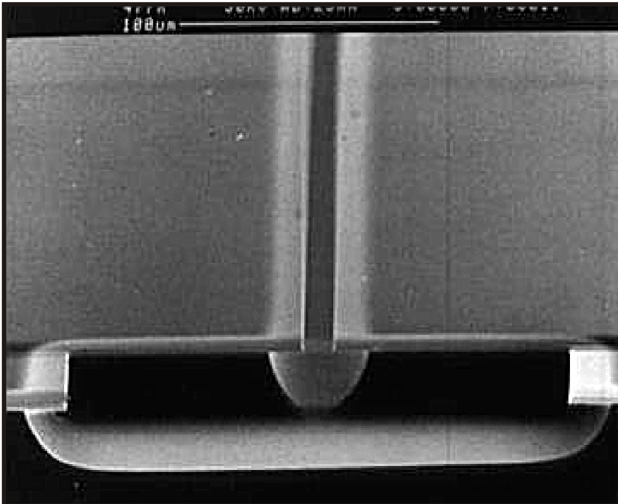
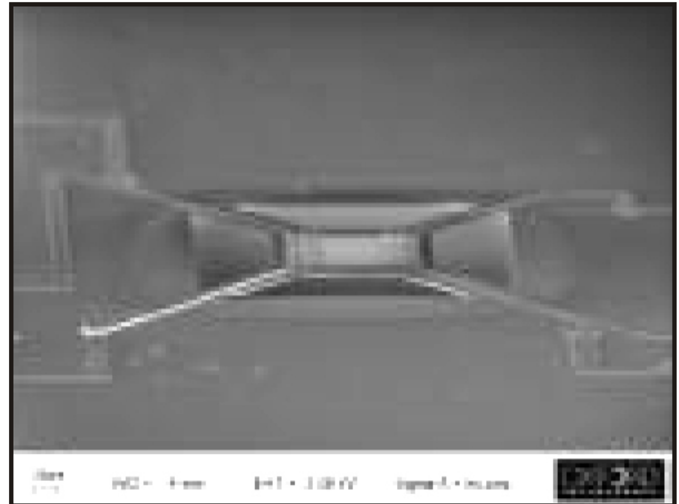
Plasmalab Data

Isotropic SI RIE

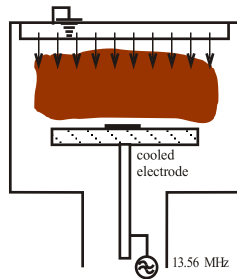


50-100 µm deep, Fluorine Etch in Si, SiO_2 mask not removed
The lower SEM shows the "microloading effect" at room temperature, (Courtesy of IMO, Wetzlar)



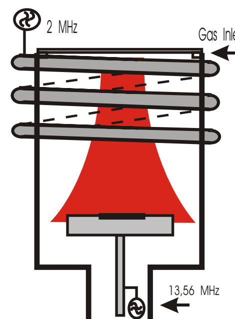
Room temperature process used to suspend the CMOS active device by removal of epi-silicon.

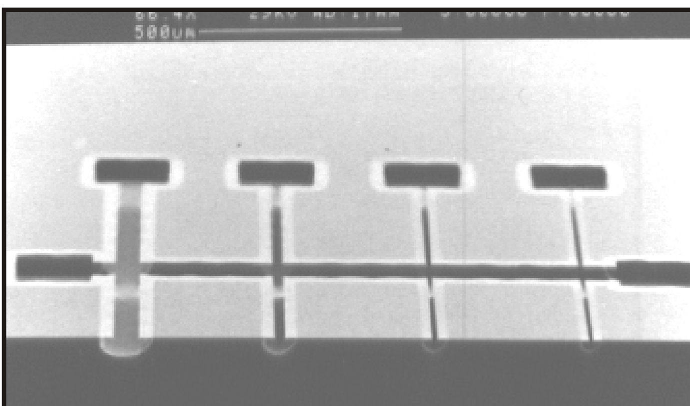
Technology:
Reactive Ion Etching or ICP - RIE
Fluor Process



Plasmalab 80 Plus
Plasmalab System 100

Plasmalab System 133





RIE Results:
Isotropic Etch
Rate : up to 4 µm / min
Uniformity: < +/- 5 % (4")
Mask: SiO_2

ICP :Rapid lateral etch
high selectivity over SiO2
process gases: SF6/O2
vertical depth: 20µm
lateral undercut: 50µm per side
lateral Si etch rate: 1.8µm/min (2x3cm chip)
selectivity Si:SiO2 > 650:1
(with ICP65)