



LPCVD of Polysilicon



By Nick Singh

Polysilicon is a designation for "polycrystalline silicon". The term polysilicon is confusing, as it does not make a distinction between microcrystalline and crystalline layers. Hence, the term polysilicon can be considered as a composite material consisting of crystalline and some amorphous Si phases. Deposition of polycrystalline silicon is an attractive technology for many applications such as liquid crystal displays, projectors, camcorders, car navigation systems, digital cameras, solar cells etc

Polysilicon is commonly deposited by the thermal decomposition or pyrolysis of silane at temperatures from 580°C –900°C. This deposition process was commercialized in the mid-1970s and has been a standard process in the microelectronics industry ever since. Commercial equipment, typically a LPCVD furnace, is available to deposit LPCVD polysilicon on different wafer sizes.

Polysilicon properties strongly depend on the deposition process and the deposition temperature, with the deposition rate exponentially increasing with temperature. The deposited films go through an amorphous – crystalline transition phase around 580°C – 620°C temperature range. Hence, films deposited in the transition region of this temperature range can show drastic changes in the crystallinity, the morphology and the optical properties and are particularly suitable for solar cell applications for example.

MOTIVATION:

The main thrust of this project work is to extend the deposition capability of the *Plasmalab System 100* PECVD by exploring the possibility of depositing crystalline silicon compounds such as polycrystalline silicon, silicon carbide and silicon germanium. The first stage of this work has focused on obtaining crystalline silicon growth at temperatures < 650°C with film properties similar to those that would be obtained in a commercial LPCVD reactor.

EXPERIMENTAL

The *Plasmalab System 100* PECVD, has been used for depositing polysilicon. The *Plasmalab System 100* PECVD is a single wafer load locked system, fitted with a patented (British Patent Application 0329460.0) new electrode design capable of operating reliably up to 650°C. 100 mm bare reclaimed silicon wafers of ~500 μm thickness, type n, < 1 0 0 > have been used as the

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substrate. The wafer is heated to the pre-set process temperature and a thin SiO₂ layer about 200 nm thick, having a refractive index of 1.46, is deposited as a sandwich layer on the wafer. The oxide film is deposited using a high temperature PECVD process. The polysilicon films have been deposited using predefined process conditions using silane as the main process gas. X ray diffraction (XRD) and Raman spectroscopy have been used to characterize the polysilicon films.

RESULTS:

Polysilicon was deposited using silane in the temperature range 550 – 700°C. The temperature dependence (figure 1) is exponential and follows the Arrhenius equation: $R=A \exp (-qE_a/kT)$ where R is the deposition rate, A is the frequency factor, q is the electronic charge, E_a is the activation energy, k is the Boltzmann's constant, and T is the absolute temperature. From figure 1, the activation energy calculated from the slope of the plot is ~1.7eV in the 600 – 700°C range and, it would appear that the reaction has not yet reached the mass transport limited regime for the process pressure and silane diluted flow conditions used. The linear portion of the graph show the surface reaction limited conditions, that the rate of reaction is slower than the rate of reactant arrival.

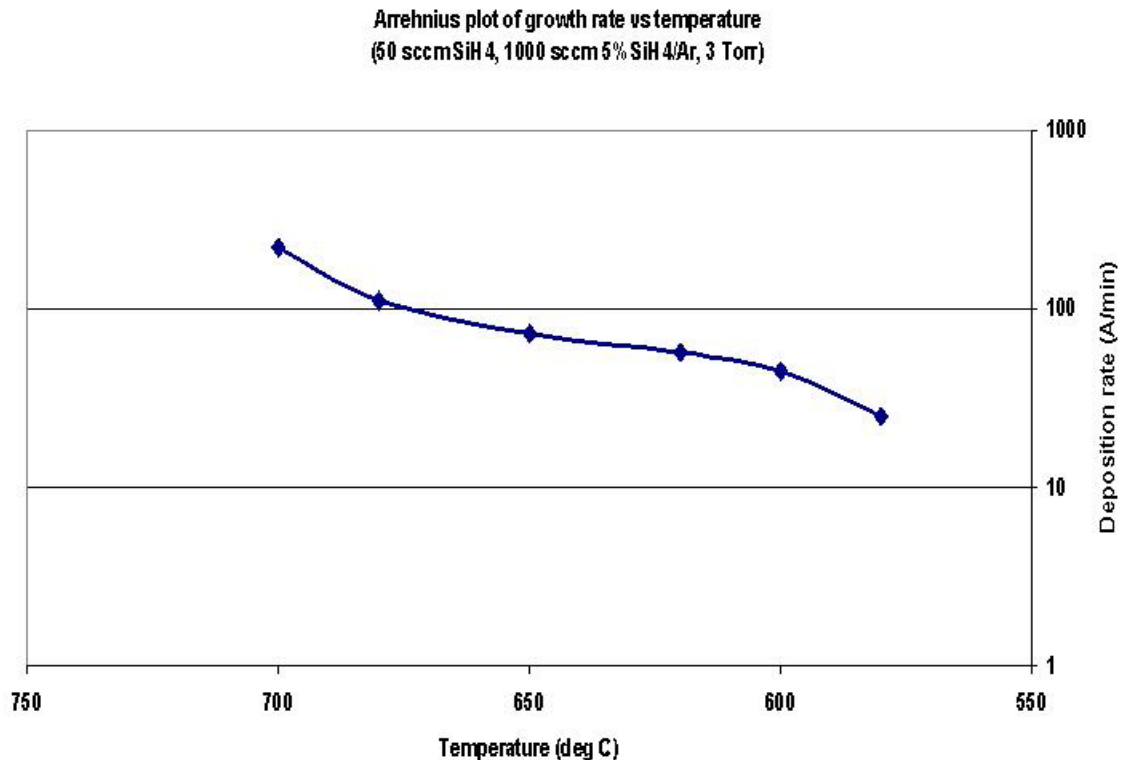


Figure 1: Arrhenius plot of deposition rate vs temperature

As shown in figure 2, a transition from amorphous to polycrystalline silicon is observed to occur around 600°C through this mixed phase regime, as the deposition temperature increases and / or the deposition rate decreases. For such films deposited slightly below the transition temperature, each layer of

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the film is deposited in an amorphous form and crystallizes as the deposition proceeds because of the lower energy of the polycrystalline structure. Nucleation of crystallites is most likely to occur by heterogeneous nucleation at the lower silicon-silicon dioxide interface. Crystallization of the amorphous silicon proceeds from these initial nuclei, with the crystalline region propagating upwards into the film by solid phase epitaxial growth. When the crystallization rate is less than the deposition rate, only the lower portion of the film (starting from the silicon-silicon dioxide) interface crystallizes during deposition, even though the crystallization process continues during the subsequent heating after the silane is turned off. Thus the silicon film can be crystalline near the interface and amorphous near the top surface, resulting in a very smooth surface. In general, the micro-structure of as-deposited silicon films is determined by the balance between the incident atom flux and the surface mobility of the adsorbed surface species. When conditions are such as the former rate is much larger than the surface mobility of the species, an amorphous like structure will develop. In contrast, in the opposite case, a polycrystalline structure will be favoured [A T Voutsas and M K Hatalis *J Electrochem Soc* 139 2659 (1992)]

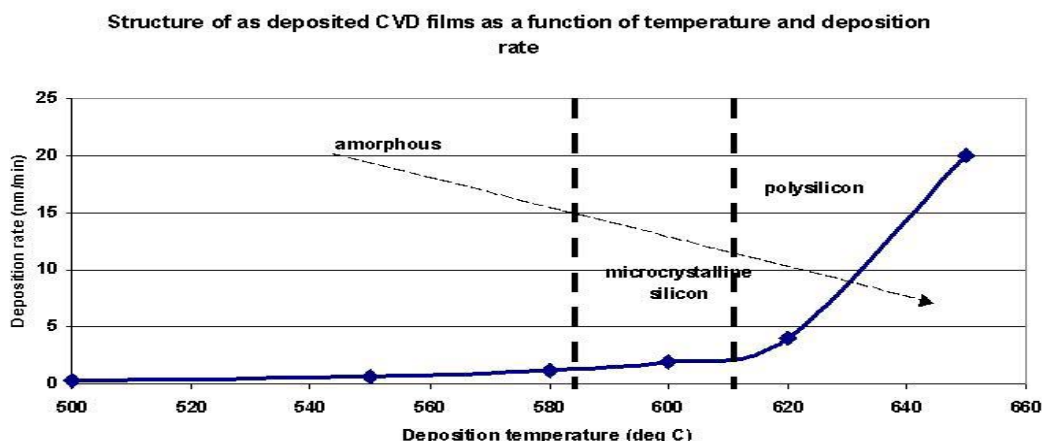


Figure 2: Structure of as deposited Si films versus temperature and deposition rate

The Raman spectrum for the transition temperature 600°C is shown in figure 3. Raman spectra show a narrow band due to crystalline silicon at 520 cm^{-1} , a slightly broader band of crystalline silicon at 950 cm^{-1} and a broader band of lower peak intensity due to amorphous silicon (483 cm^{-1}) overlapping on the wings of the 520 cm^{-1} . No other amorphous silicon peaks, 330 cm^{-1} and 445 cm^{-1} , are present. The SiH peak, 630 cm^{-1} is also absent. In our case, the FWHM is less than 40 cm^{-1} corresponding to a mixed phase material, such as microcrystalline silicon obtained at 600°C. This structure contains small crystalline regions, which give rise to a dispersion of the crystalline TO mode to lower frequencies (The broadened asymmetric Raman peak, slightly downshifted from 520 cm^{-1}) as observed in figure 3. Crystalline size influences the Raman position, i.e., peak position is a measure for crystalline size in the poly-Si. For example, in figure 3, the peak is downshifted by about 2 cm^{-1} with respect to the reference sample corresponding to an average crystalline size of 30nm

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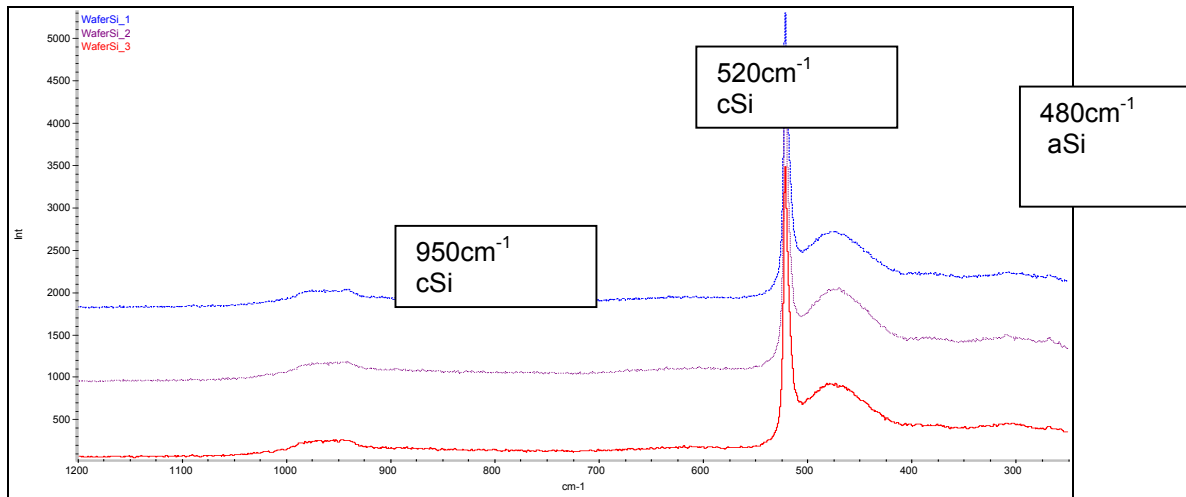


Figure 3: Microcrystalline growth at transition temperature: combination of crystalline structures and amorphous pockets.(measured at 3 different positions across the wafer)

CVD films deposited at 650°C showed the presence of a sharp 520 cm⁻¹ peak indicative of crystalline silicon growth (figure 4). The 520 cm⁻¹ bands of all the polycrystalline silicon samples overlay those of the crystalline reference sample, so it is hard to see that there is a shoulder here. The slight increase in the wings could be due to tiny fragments of amorphous tissue. Overall, this clearly shows crystallinity of the samples and a high degree of crystallinity for all the samples. The estimated grain size based on the shift of 520 cm⁻¹ peak at 650°C is > 100 nm (10 nm - 300 nm across the 600 – 700°C temperature range) comparable to literature. The degree of crystallinity at 650°C is estimated to be > 80%

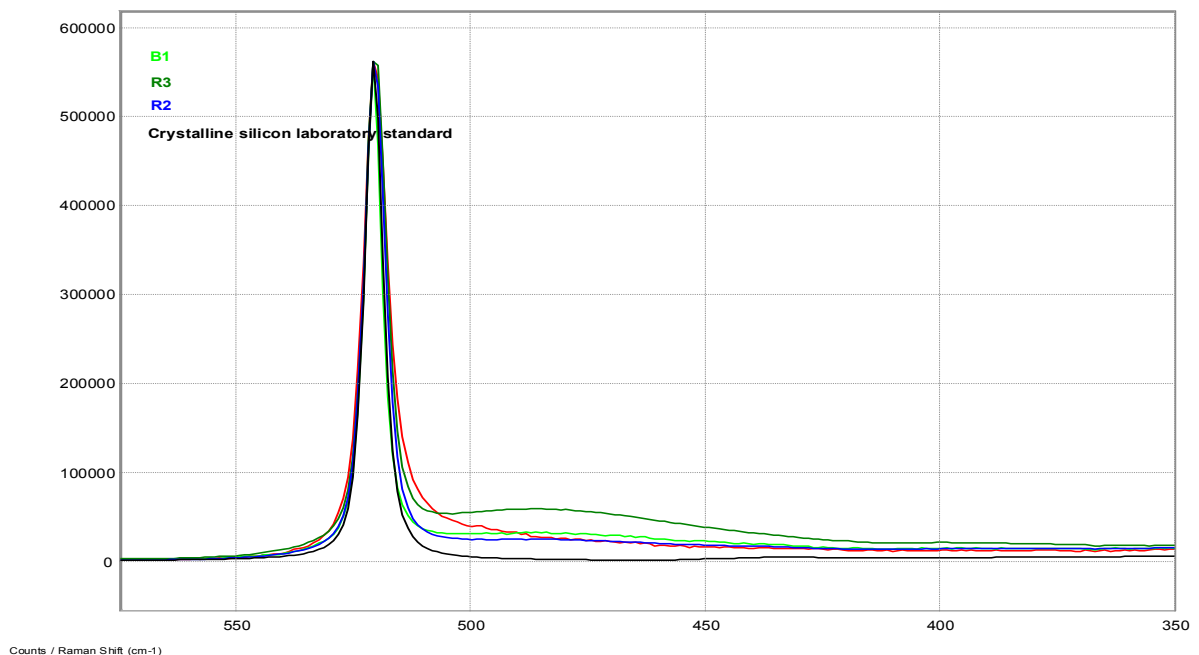


Figure 4: Raman spectra limited to 575-350 cm⁻¹, and normalised to peak height at 521 cm⁻¹.

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Figure 5a shows the diffraction peaks obtained using the glancing angle XRD diffraction method. (1 1 1), (2 2 0) and a weak (3 1 1) peaks have been obtained. The polysilicon film grows preferentially along the (2 2 0) and hence (1 1 0) orientation during deposition at 650°C. Peak intensity of (1 1 1) is higher than (2 2 0). Figure 5b shows the effects of annealing; after annealing (1 1 1) and (3 1 1) orientation increased while (2 2 0) orientation stayed the same. This indeed indicates a change in the microstructure as the polysilicon film is further crystallized due to annealing, but mainly along certain directions. The fact that high temperature annealing does not influence the intensity of the (2 2 0) peak indicates that almost no rotation of the crystal structure from (2 2 0) to (1 1 1) takes place during annealing. The higher (1 1 1) peak indicates that recrystallization of polysilicon occurs along (1 1 1) orientation.

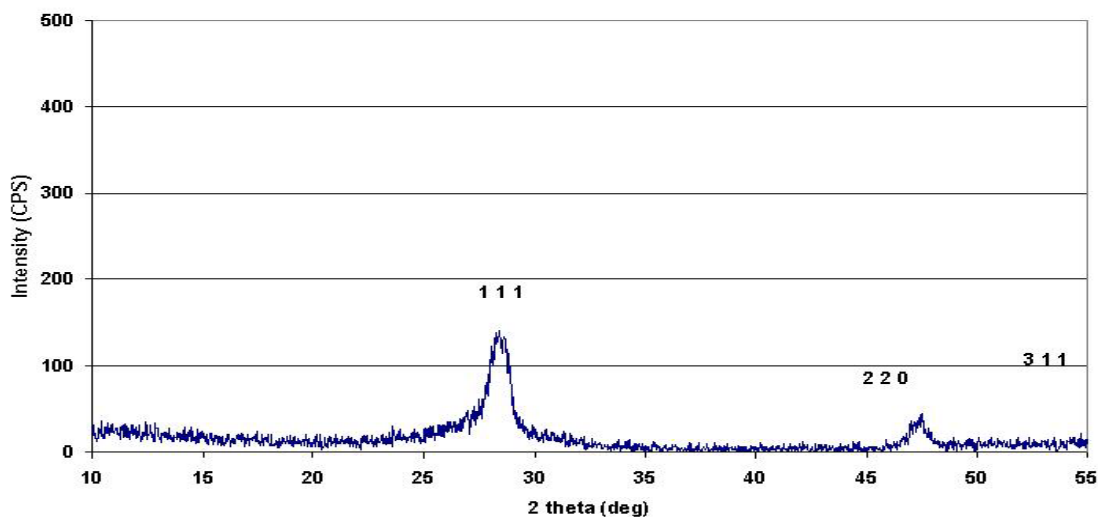


Figure 5a: Before anneal

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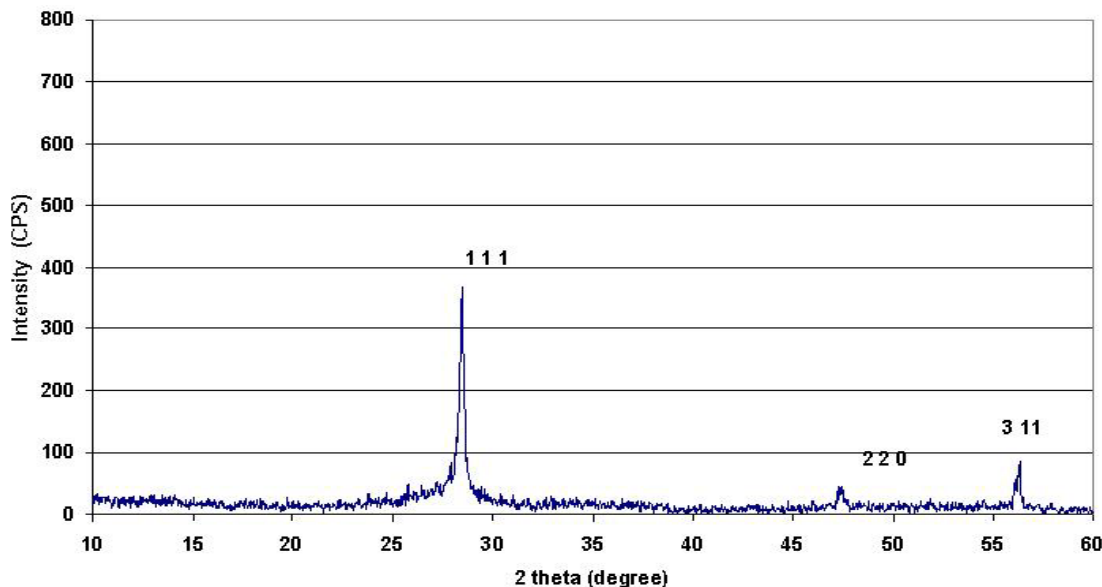


Figure 5b: After anneal

The width of the measured XRD peaks is determined by the size of the crystallites. The average diameter of the crystallites with a certain orientation can therefore be estimated from the corresponding XRD peak using Scherrer's formula.

$$t = \frac{0.9\lambda_{X-ray}}{B \cos \theta_B}$$

where B is the full width at half maximum of the measured peak

in radians, and θ_B the peak angle. Figure 6 shows a normalized XRD signal as a function of temperature for polycrystalline silicon film about 2 μm thick deposited on a 200 nm SiO₂ layer on a 100 mm silicon wafer at 500 mTorr. The deposition rate was 10 nm/min. XRD shows preferred orientation in the highly peak (1 1 0), (2 2 0) peak increases with temperature. (2 2 0) peak is expected to be higher than the (1 1 0) and dominate at higher temperatures according to literature. The degree of crystallinity is estimated to be > 80%.

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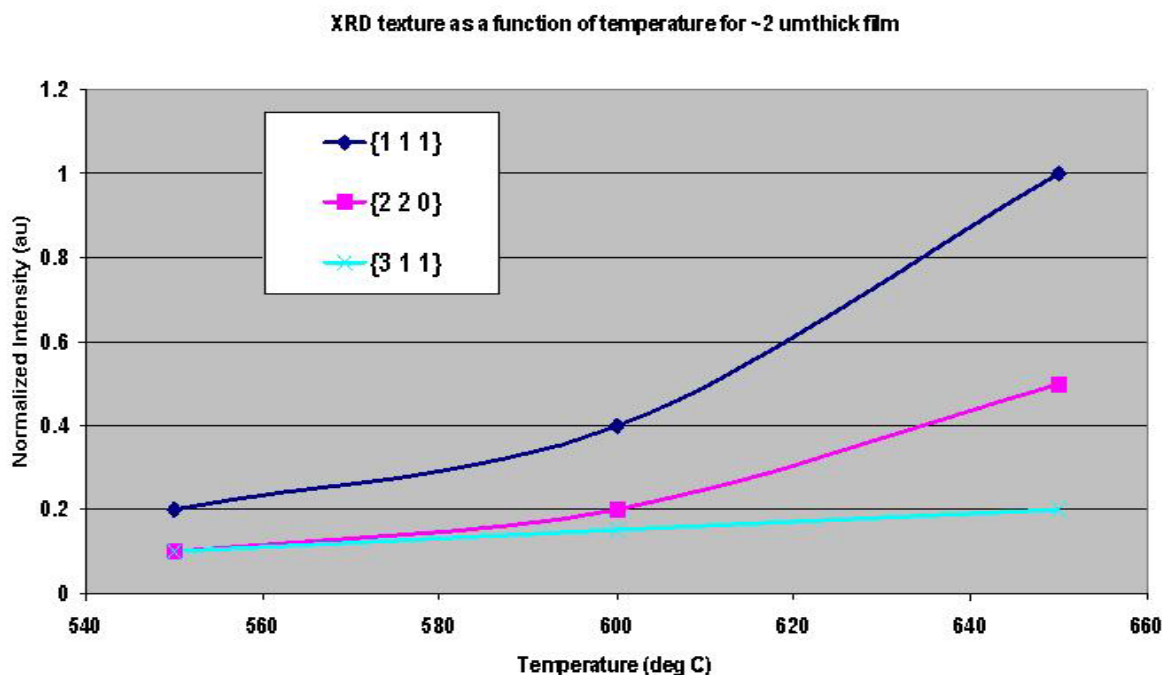


Figure 6: XRD texture as a function of temperature for 2 μm thick polycrystalline silicon film

CONCLUSION

The Oxford Instruments Plasma Technology *Plasmalab System 100* is capable of depositing polycrystalline silicon at 650°C. Growth rates > 40 nm/min and film thickness uniformity < +/- 2 % across 100 mm wafer has been achieved for LPCVD process conditions.

XRD and Raman analysis of the as deposited films demonstrate the crystalline nature of the films: grain sizes > 100 nm and a degree of crystallinity > 80%. The polysilicon films grow preferentially along <1 1 0> orientation and crystallization occurs along <1 1 1> orientation.